

Official

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Please amend the paragraph on page 83, line 24 to page 84, line 15 as follows:

A2
Fig. 1 is a block diagram showing an example of a shift register circuit according to the present invention. This shift register circuit 11 is constructed by serially connecting a plurality of latch circuits (half latch circuits) LAT. That is, a start signal (pulse signal) st is inputted to the input node of the latch circuit LAT of the first stage, while the input node of the latch circuit LAT of the second stage is connected to the output node. Likewise, the input node of each latch circuit LAT is connected to the output node of the preceding stage, while the output node is connected to the input node of the latch circuit LAT of the succeeding stage. Then, a clock signal ck is inputted to the control nodes of the latch circuits LAT of the odd-number stages. In contrast to this, a clock signal /ck that is the inverted signal of the clock signal ck is inputted to the control nodes of the latch circuits LAT of the even-number stages.

Please amend the paragraph on page 85, lines 3-12 as follows:

A3
Fig. 2 shows a circuit diagram showing an example of the construction of a latch circuit that constitutes the shift register circuit 11 of Fig. 1. To the source electrodes of two p-type transistors M11 and M12 that serve as first and second p-type transistors is connected a power potential Vcc (=16 V). Then, the gate electrode of the p-type transistor M11 is connected to the drain electrode of the p-type transistor M12, while the gate electrode of the p-type transistor M12 is connected to the drain electrode of the p-type transistor M11.

Please amend the paragraph on page 86, lines 20-24 as follows:

A4
Fig. 3 shows a latch circuit LAT that serves as an example of a shift register circuit constructed by incorporating the first and second clock signal input sections 12 and 13 to the latch circuit of Fig. 2.

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Please amend the paragraph on page 92, lines 16-17 as follows:

A5 Fig. 5 shows another example of a latch circuit according to the present invention.

Please amend the paragraph on page 95, lines 19-20 as follows:

A6 Fig. 7 shows another example of a latch circuit according to the present invention.

Please amend the paragraph on page 96, lines 9-10 as follows:

A7 Fig. 8 shows another example of a latch circuit according to the present invention.

Please amend the paragraph on page 97, lines 10-13 as follows:

A8 Fig. 9 shows an example of a latch circuit constituting the logical product and non-disjunction circuits AND-NOR1 and AND-NOR2 shown in Fig. 8.

Please amend the paragraph on page 98, lines 6-7 as follows:

A9 Fig. 10 shows another example of a latch circuit according to the present invention.

Please amend the paragraph on page 99, lines 4-6 as follows:

A10 Fig. 11 shows an example of a latch circuit constituting the first and second non-conjunction circuits NAND1 and NAND2 shown in Fig. 10.

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Please amend the paragraph on page 99, lines 18-19 as follows:

A11

Fig. 12 shows another example of a latch circuit according to the present invention.

Please amend the paragraph on page 100, lines 6-7 as follows:

A12

Fig. 13 shows another example of a latch circuit according to the present invention.

Please amend the paragraph on page 101, lines 12-13 as follows:

A13

Fig. 15 shows another example of a latch circuit according to the present invention.

Please amend the paragraph on page 102, lines 17-18 as follows:

A14

Fig. 16 shows another example of a latch circuit according to the present invention.

Please amend the paragraph on page 103, lines 12-13 as follows:

A15

Fig. 17 shows another example of a latch circuit according to the present invention.

Please amend the paragraph on page 104, lines 22-23 as follows:

A16

Fig. 18 shows another example of a latch circuit according to the present invention.

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Please amend the paragraph on page 106, lines 5-7 as follows:

A17 Fig. 19 shows an example of the first clock signal input control section 12 of a shift register according to the present invention.

IN THE CLAIMS

Please amend claims 1, 18, and 37 as follows:

Sub B1
A18 1. (Amended) A latch circuit for synchronizing a pulse signal with a clock signal, comprising:
a first input comprising the pulse signal;
a second input comprising the clock signal; and
an output comprising the pulse signal in synchronization with the clock signal, wherein the clock signal has an amplitude smaller than an amplitude of the pulse signal outputted from the latch circuit.

A19 18. (Amended) A shift register circuit having a plurality of latch circuits for transmitting a pulse signal in synchronization with a clock signal, each of the latch circuits comprising:
a clock signal input control section for executing control to input and stop the supplied clock signal, wherein the clock signal has an amplitude smaller than an amplitude of the pulse signal; and
an output comprising the pulse signal in synchronization with the clock signal.

A20 37. (Amended) A CMOS logical circuit which performs a logical operation based on a plurality of input signals, the CMOS logical circuit comprising:
a first input signal having a first amplitude; and
a second input signal having a second amplitude;
wherein the amplitude of at least one of the input signals is smaller than a drive voltage of the CMOS logical circuit.

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Please add the following new claims:

61. (New) An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the logical circuit as claimed in claim 37 is used as a logical circuit receiving an output pulse of a shift register circuit constituting the data signal line drive circuit and a pulse width control signal inputted from outside as input signals and generating an output signal having a pulse width smaller than the pulse width of the output pulse of the shift register circuit.

A21 62. (New) An image display device as claimed in claim 61, wherein in the logical circuit constituting the data signal line drive circuit and the scanning signal line drive circuit, an output signal of the shift register circuit is inputted to a gate electrode of the transfer transistor.

63. (New) An image display device comprising: a plurality of pixels arranged in the shape of a matrix such that the pixels are surrounded with a plurality of data signal lines arranged in a direction of column and a plurality of scanning signal lines arranged in a direction of row; a data signal line drive circuit for supplying a video signal to the data signal lines; and a scanning signal line drive circuit for supplying a scanning signal to the scanning signal lines, wherein

the logical circuit as claimed in claim 37 is used as a logical circuit receiving an output pulse of a shift register circuit constituting the scanning signal line drive circuit and a pulse width control signal inputted from outside as input signals and generating an output signal having a pulse width smaller than the pulse width of the output pulse of the shift register circuit.